

## REMARKS

Claims 1, 4, 5, 13, 14, 16 and 19 have been amended and claims 10 to 12, 15, 17 and 18 have been canceled. Claims 4, 5, 7, 13, 14 and 16 were objected to and claim 20 was allowed. Claims 1 to 9, 13, 14, 16, 19 and 20 remain active in this application of which claims 4, 5, 7, 13, 14, 16 and 20 have been allowed or indicated to be allowable. Allowable claims 4, 5, 14 and 16 have been rewritten in independent form with minor cosmetic amendment and should now be allowed along with previously allowed claim 20. Please charge any costs to Deposit Account No. 20-0668.

Claims 1 to 3, 6, 8 to 12, 15 and 17 to 19 were rejected under 35 U.S.C. 102(e) as being anticipated by Gulati et al. (U.S. 6,686,860). The rejection is respectfully traversed.

Claim 1 relates to a method for reconfiguring an analog-to-digital converter and requires, among other steps, providing an analog-to-digital converter having a plurality of serially connected stages and an input terminal, each stage including a switchable integrator capable of operation as one of a sample/hold circuit and as an integrator. No such step is taught or suggested by Gulati et al. either alone or in the combination as claimed.

Claim 1 further requires the step of receiving at the analog-to-digital converter a control signal and, at the input terminal, an input analog signal, the control signal having a state selected from a group consisting of a first state and a second state, the first state associated with a first configuration of the stages by causing the switchable integrator to operate as a sample/hold circuit, the second state associated with a second configuration of the stages by causing the switchable integrator to operate as an integrator, the input

analog signal comprising information. No such step is taught or suggested by Gulati et al.

Claims 2, 3 and 6 to 9 depend from claim 1 and therefore define patentably over the applied reference for at least the reasons presented above with reference to claim 1.

Claim 7 further limits claim 1 by requiring that processing the digital signal to generate a digital output further comprises decimating the digital signal to yield an averaged digital signal, the averaged digital signal having a higher resolution than the digital signal and filtering the averaged digital signal to yield the digital output. No such step is taught or suggested by Gulati et al. either alone or in the combination as claimed.

Claim 19 requires, among other features, an analog-to digital converter having a plurality of serially connected stages and input terminal, each stage including a switchable integrator capable of operation as one of a sample/hold circuit and as an integrator. No such structure is taught or suggested by Gulati et al. either alone or in the combination as claimed.

Claim 19 further requires means for receiving at the digital-to-analog converter a control signal and, at the input terminal, an input analog signal, the control signal having a state selected from a group consisting of a first state and a second state, the first state associated with a first configuration of the stages by causing the switchable integrator to operate as a sample/hold circuit, the second state associated with a second configuration of the stages by causing the switchable integrator to operate as an integrator, the input analog signal comprising information. No such structure is taught or suggested by Gulati et al. either alone or in the combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



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